Fine Pitch High Bandwidth Flip Chip Package-on-Package Development

by

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***Abstract*—As the demands of higher performance, higher bandwidth, lower power consumption as well as multiple functions increases in mobile applications, the mobile phone has evolved from a simple communication device to a complicated and highly integrated system with multiple functions and heterogeneous devices. Due to the fast growth in emerging markets for mobile applications, packaging technology has become more challenging than ever before, driving advanced Silicon (Si) nodes, finer bump pitch as well as finer line width and spacing substrate manufacturing capabilities to satisfy the increasing requirements in mobile devices. Flip chip chip scale package (fcCSP) is viewed as an attractive solution when higher input/output (I/O) counts in a package are needed. In order to enhance the performance, reduce the power consumption and increase transition rates, three-dimensional (3D) package-on-package solution with flip chip interconnect (fcPoP) has been widely utilized to successfully achieve these goals. With the ability to stack a logic processor and low power double data rate (LPDDR) memory device in a single package, the utilization of fcPoP is becoming a preferred solution in the mobile market segment for a better power and performance balance. However, as more and more functions are designed in a chip to target the high-end mobile market, the die is becoming larger and larger. With the larger die size, it is challenging for the regular fcPoP structure to support high bandwidth top memory I/O counts in a limited package size. In order to solve the constraints of larger die and/or package size limitations, top memory with wide I/O counts as well as customized mobile memory applications, high bandwidth fcPoP technology is proposed as an strong solution. This paper reports the development of a fine pitch high bandwidth fcPoP. The top interposer substrate with copper (Cu) post interconnections peripherally is connected to bottom package. The top interposer substrate can be designed in a different top and bottom pitch to connect top mobile memory and bottom packages, respectively. With this structure, die size limitations can be overcome by using finer interconnection pitch, providing the flexibility to allow any memory interface pitch application. In addition, through this developed result, not only the package warpage/coplanarity control and reliability characterization are illustrated, it also demonstrated this enabling technology of high bandwidth fcPoP as a highly integrated, miniaturized and low profile 3D packaging solution.**

Keywords— flip chip package; high bandwidth package-on-package; interposer; Copper post; 3D package

I. INTRODUCTION

Emerging markets are always driving demand for higher performance, higher bandwidth, lower power consumption as well as increasing functionality in mobile applications. Packaging technology has become more challenging and complicated than ever before, driving advance Silicon (Si) nodes, finer bump pitch as well as finer line width and spacing substrate manufacturing capabilities to satisfy the increasing requirements in the semiconductor industry. As increasing input/output (I/O) counts in a package are needed in mobile devices, packaging solutions are migrating from traditional wire bond packages to flip chip interconnect to meet these requirements. Flip chip chip scale package (fcCSP) is viewed as an attractive solution for complicated and highly integrated systems with multiple functions and heterogeneous mobile applications [1, 2]. Due to the fast growth in emerging markets for mobile applications, a numbers of wireless devices have jumped to the 4G Long Term Evolution (LTE) communication platform and may ramp to 5G wireless technology in the next two to three years. In addition, advanced silicon (Si) node (14/12/10nm and below) technology development in mobile applications can pursue the die size reduction, efficiency enhancement and lower power consumption. For the purpose of having the shortest interconnection between logic devices and mobile low power double data rate (LPDDR) memory, three-dimensional (3D) package-on-package solutions with flip chip interconnect (fcPoP) has been widely utilized. With the ability to stack a logic processor and memory device in a single package, the utilization of fcPoP is becoming a preferred solution for achieving the best performance and efficiency as well as smaller form factor in the mobile market segment [3-5].

Although fcPoP is becoming a preferred solution in the mobile market segment for a better power and performance balance, the scaling of die size in fcPoP is also an important topic when more and more functions are designed in a chip to target the high-end mobile market. With the larger die size, it is challenging for the regular fcPoP structure to support top memory I/O counts of more than 350 I/O in a limited package size (like 14x14 or 15x15mm). In addition, memory packages with wide I/O counts (more than 500 I/O) are also expected to be the future trend in emerging market applications. Hence, the high bandwidth fcPoP technology becomes a strong solution to

solve the constraints of larger die and/or package size limitations, top memory with wide I/O counts as well as customized mobile memory applications [6]. Moreover, since emerging markets are driving advanced technologies in high performance mobile devices, assembly cost is still the major issue to be addressed. As the substrate cost is always the significant factor in a flip chip package, flip chip assembly with a low cost substrate has become a hot topic in the industry. The flip chip interconnect with Cu pillar bond-on-lead (BOL) structure on embedded trace substrate (ETS) has been widely adopted for low cost demand. The flip chip interconnect with Cu pillar BOL and enhanced processes (fcCuBE®) can also help to deliver a high performance packaging solution with a cost effective mass reflow (MR) manufacturing process [7]. Therefore, in order to develop the technology of a fine pitch high bandwidth fcPoP, a test vehicle of package size around 200mm^2 with a top interposer substrate that interconnects the top mobile memory and bottom package peripherally by using Cu posts was evaluated in this paper, which the schematic is shown in Fig. 1. Different top and bottom ball pitch to connect top mobile memory and bottom packages can be designed in this utilized top interposer substrate. The fine Cu post pitch of 0.23mm on an interposer (connects to bottom substrate) and solder ball pitch of 0.35mm on the bottom substrate (connecting to printed circuit board) was utilized. With this high bandwidth fcPoP structure, die size limitations can be overcome by using this finer interconnection pitch, providing the flexibility to allow any memory interface pitch application. Furthermore, through this developed result, it not only illustrated this package can meet warpage and coplanarity targets but also can pass the long term package reliability conditions without any failure observed. It shows that this high bandwidth fcPoP architecture is an enabling technology for highly integrated, miniaturized, low profile and cost-effective 3D packaging solutions.

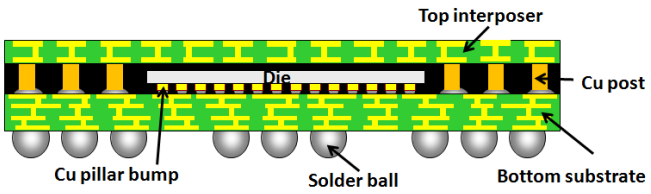


Fig. 1. Schematic of a high bandwidth fcPoP

II. Characterization of High Badnwidth fcPoP

As the fcPoP stacks fully tested memory and logic packages to eliminate known good die (KGD) issues, it provides flexibility in mixing and matching IC technologies and enables assembly of larger dies in a thinner PoP stack up with finer top ball pitch. The fcPoP is typically adopted as the ideal solution with its overmold configuration that provides better warpage performance and drives aggressive package height reductions and finer mobile memory pitch down to 0.4mm and below. The surface treatment of CuOSP on the bottom substrate and top memory interface pads is typically utilized and can support down to 0.3mm minimum ball pitch on bottom/BGA pads and much finer pitch on top memory interface pads of the bottom package. Both capillary underfill (CUF) and molded underfill (MUF) are available in fcPoP, although MUF technology allows for increased cavity size and larger die size with a lower assembly cost solution. However, the continued demands for higher level integration has led the industry to evaluate new fcPoP technologies to be utilized with stacking of wide I/O counts and/or next generation mobile memory. The high bandwidth fcPoP technology is one of the new technology solutions to achieve these goals, featuring a top interposer substrate that interconnects the top mobile memory and bottom package peripherally by using Cu post, Cu cored solder ball (CCSB) [8, 9], solder ball [10], etc. In order to develop the technology of high bandwidth fcPoP with Cu post architecture, a test vehicle with package size of ~200mm^2 was utilized. The die size of 75mm^2 and die thickness of 65µm as well as minimum 80µm Cu pillar bump pitch was evaluated. A two-layer (2L) cored substrate with total thickness of 0.11mm was used as top interposer. The Cu posts with 0.23mm pitch, 0.15mm height and 0.12mm diameter were manufactured in this interposer. Thin package profile high bandwidth fcPoP is an important topic in the industry as it added a top interposer substrate increasing fcPoP height. Due to the benefit of total stiffness enhancement with the use of top interposer substrate, a thinner bottom substrate can be utilized to compensate the package height increment. Even though the thinner bottom substrate adoption may result in larger warpage and coplanarity, it still can be compensated with the use of a top interposer substrate. Hence, for the purpose of reducing the package profile and driving finer solder ball pitch, the four-layer (4L) coreless ETS of 0.17mm substrate thickness (with 25/25/25µm prepreg thickness) and 0.35mm bottom solder ball pitch was also estimated in this test vehicle. With the structure stack-up analysis, the maximum total package thickness of this high bandwidth fcPoP can meet less than 0.63mm. Fig. 2 illustrates the assembly process flows of this examined high bandwidth fcPoP.

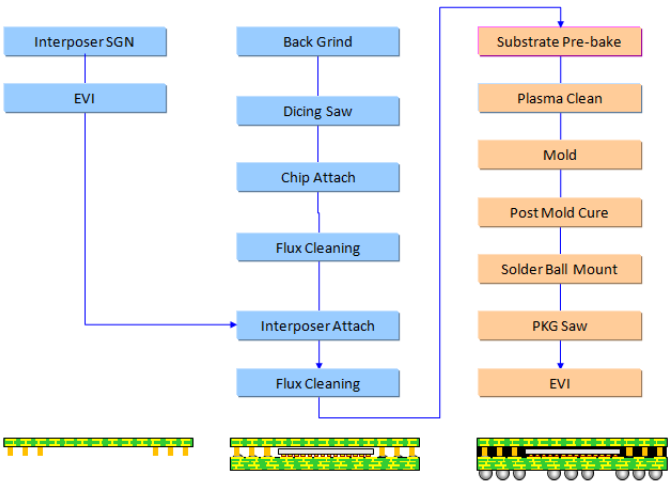
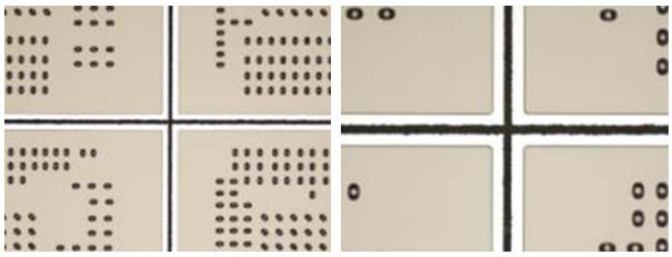


Fig. 2. Assembly process flow for high bandwidth fcPoP

Fig. 3 illustrates the visual inspection image of Kerf width in die preparation (DP) process, which indicates that the Kerf width meets the specification of maximum 45µm. Fig. 4 shows the X-ray inspection result after chip attach (CA) process,

which is clearly illustrated that there is no abnormality of solder bridge phenomenon observed during the CA process. Fig. 5 illustrates the X-ray inspection result after top interposer attach process, which shows that there is no any abnormality of solder bridge and non-wet phenomena found during this process. In addition, these results also illustrate the accuracy of Cu pillar bumps and/or Cu posts alignment and robust flip chip assembly technology with MR that was examined in this high bandwidth fcPoP structure. Fig. 6 illustrates the C-Mode Scanning Acoustic Microscopy (C-SAM) inspection result after MUF process for this high bandwidth fcPoP and shows that there was no abnormality of MUF void or delamination observed.



-. Meet the Spec criteria.

Fig. 3. Visual inspection for Kerf width in DP process

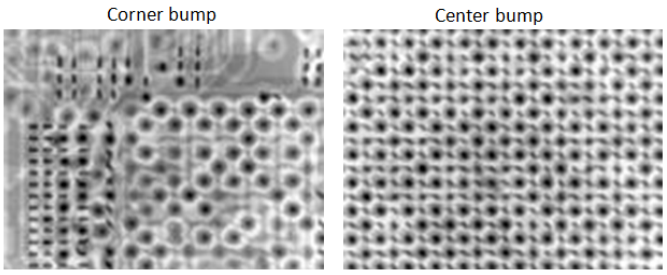
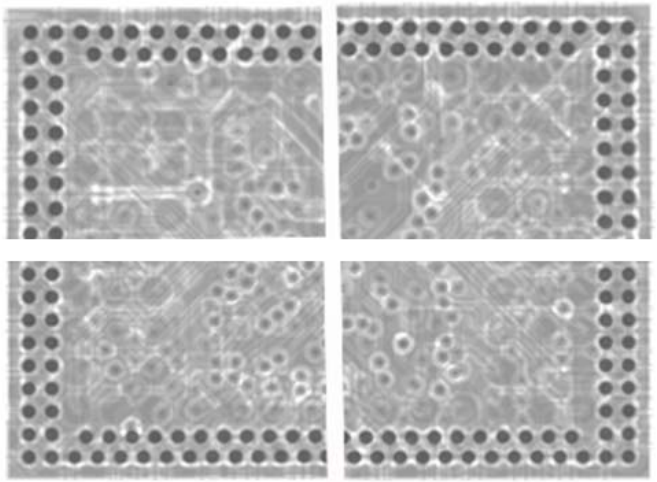
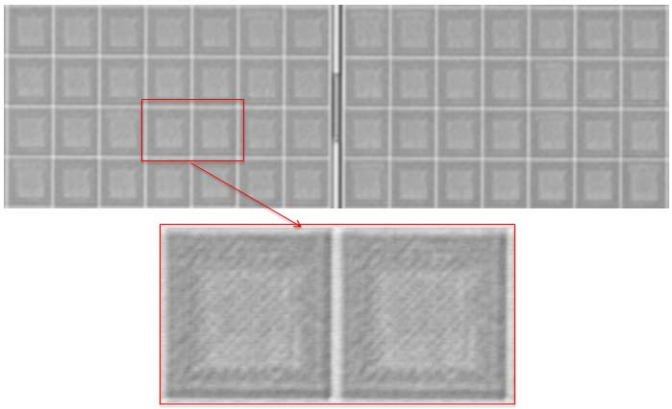


Fig. 4. X-Ray inspection after CA process



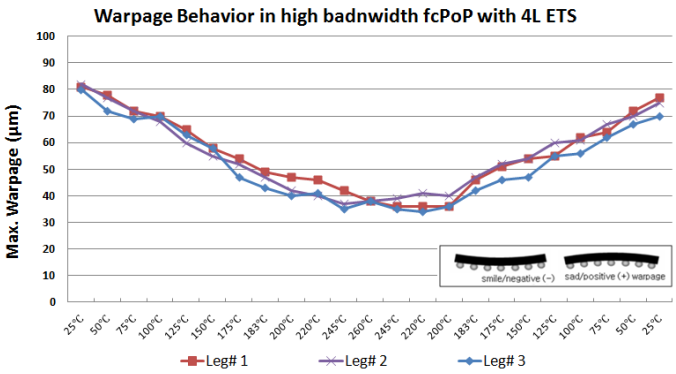
-. Accuracy alignment for interposer attach
-. No abnormality of solder bridge and non-wet was found.

Fig. 5. X-Ray inspection after top interposer attach process

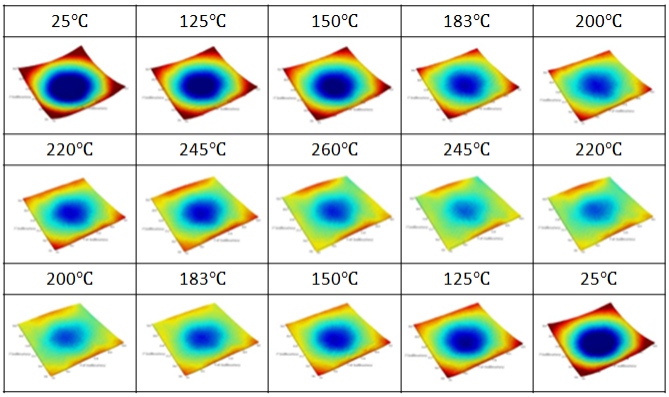


-. No abnormality was found by C-SAM inspection after Mold process

Fig. 6. C-SAM inspection after MUF process



(a)



(b)

Fig. 7. Warpage behavior for high bandwidth fcPoP (a) maximum warpage distribtuion plot; (b) 3D warpage contour plot.

Fig. 7 (a) shows the warpage distribution for this high bandwidth fcPoP with 4L ETS while Fig. 7 (b) illustrates the 3D warpage contour plots. From Fig. 7, it was found that this structure shows the warpage behavior trend of cry-cry-cry shapes instead of the typical warpage behavior trend cry-smile-cry shapes in fcCSP [11]. However, all three legs still can meet the warpage specification of less than 80µm at every temperature read point and the maximum warpage can be reduced to less than 40µm at high temperature. With the observed small value of maximum warpage in this high

bandwidth fcPoP, it can reduce the non-wet risk in Surface Mount Technology (SMT) processes and guarantee the good yield performance after SMT. In addition, through the coplanarity assessment illustrated in Fig. 8, it was found that all three legs shows good coplanarity less than 90µm and good Cpk values greater than 2.0. It also indicates that the process is consistently under control with higer Cpk value. For the purpose of measuring total package height, the cross-sectional image of this high bandwidth fcPoP was illustrated in Fig. 9, which indicates the average package height is around 596µm (without stacking top memory). Moreover, through the cross sectional inspection, it also showed the good Cu pillar bump and Cu post interconnection joints after assembly processes.

Leg	Die thickness	Min.	Max.	Avg.	Std.	Cpk
1	65µm	30	88	52.9	8.64	2.59
2		33	89	53.3	10.22	2.18
3		33	90	51.8	7.57	3.00

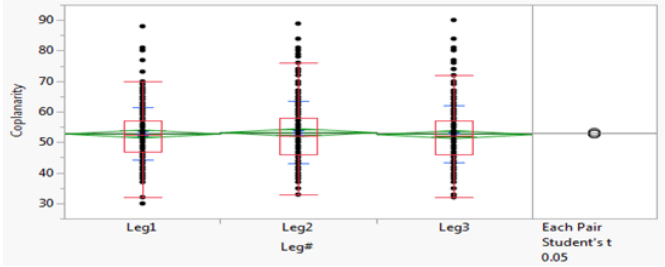
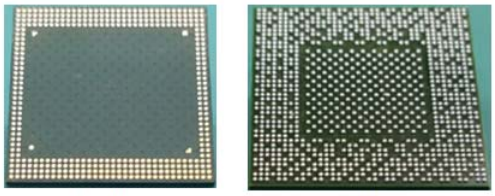


Fig. 8. Coplanarity behaviors in a high bandwidth fcPoP with 4L ETS



Item	A Interposer Thickness	B Substrate Thickness	C Bottom Ball Height	D Mold Thickness	E Die Thickness	Total PKG Height (A+B+C+D)
Average	118.3	182.3	145.3	150	65	596

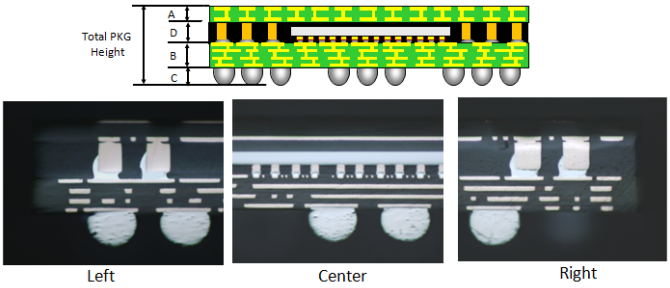


Fig. 9. Cross-sectional view in high bandwidth fcPoP

III. Long-term Reliability Test Assessment

In order to validate the package reliability of this high bandwidth fcPoP with 4L ETS, this package was evaluated in long term reliability tests such as pre-condition of moisture sensitivity level (MSL3A) as well as unbiased highly accelerated stress test (uHAST) of 96 hours (with pre-condition of MSL3A) and extended to 192 hours, thermal cycling test condition B (TCB) of 1000 cycles (with pre-condition of MSL3A) and high temperature storage test (HTST) of 1000 hours. The long-term package reliability results and images of all three legs based on utilizing Through Scanning Acoustic Microscopy (T-SAM) inspection after uHAST 192 hours, TCB 1000 cycles and HTST 1000 hours are illustrated in Fig. 10. From Fig. 10, it is observed that there is no abnormality observed through T-SAM images. In order to realize the solderability of Cu post interconnections that connect to bottom substrate, the cross-sectional images after uHAST 192 hours, TCB 1000 cycles and HTST 1000 hours that utilized Scanning Electro Microscopy (SEM) technology were shown in Fig. 11. From Fig. 11, it is clearly indicated that there is no solder bridge as well as non-wet phenomena found after the long-term reliability test. Based on these reliability test result, it not only shows that the illustrated 4L ETS high bandwidth fcPoP examined in this study can guarantee low package profile assembly without any yield loss and solder bridge, but also meet the reliability criterion. Therefore, it is believed that with the technology established in this paper for high bandwidth fcPoP can provide a highly integrated, miniaturized and low profile 3D packaging solution in semiconductor industry.

Leg#	Die Thickness	Reliability Test Results						
		MSL3A	MSL3				HTST 500hrs	HTST 1000hrs
			uHAST 96hrs	uHAST 192hrs	TCB 500x	TCB 1000x		
1	65um	0/45	0/45	0/45	0/45	0/45	0/45	0/45
2		0/45	0/45	0/45	0/45	0/45	0/45	0/45
3		0/45	0/45	0/45	0/45	0/45	0/45	0/45

-. Sample size: 45ea in each reliability test item

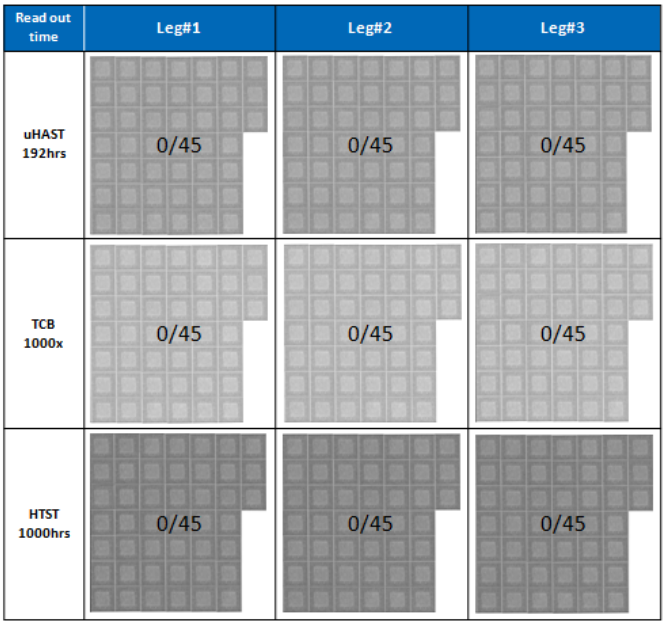
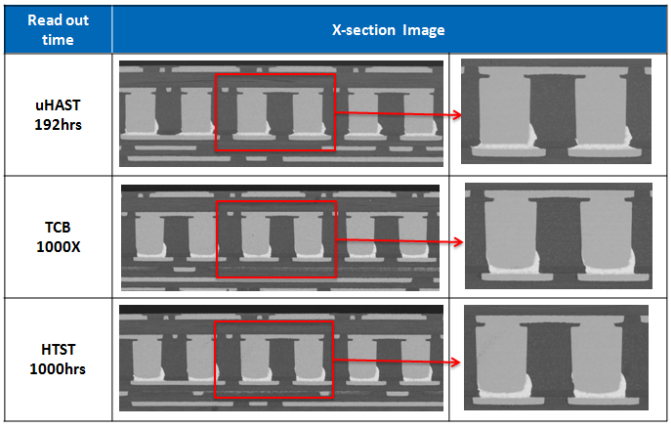


Fig. 10. Long term package reliability result and T-SAM image inspection in a 4L ETS high bandwidth fcPoP



-. No abnormality at Cu post interconnection area after reliability test (uHAST 192hrs, TCB 1000x, HTST 1000hrs) observed.

Fig. 11. Cross-sectional view in Cu post interconnectin area after long-term relibility test

IV. Conclusions

This paper reports the evaluations of a high bandwidth flip chip package-on-package (fcPoP) that features a top interposer with Cu post interconnections attach to fcPoP bottom substrate. The thinner die of 65µm thickness and coreless 4L embedded trace substrate (ETS) of 0.17mm thickness as well as finer Cu post interconnections pitch of 0.23mm and bottom solder ball pitch of 0.35mm was studied. The flip chip assembly processes such as die preparation, chip attach, mold underfilling and interposer attach processes were illustrated to show the robust and reliable process control in this high bandwidth fcPoP evaluation. The warpage and coplanarity assessments were also illustrated to show the examined high bandwidth fcPoP structure can not only meet the warpage and coplanarity specification, but can also guarantee the SMT performance to avoid high risk of non-wet phenomenon. Moreover, the utilization of thinner 4L ETS can also reduce the maximum total package height to less than 0.63mm based on the evaluation result (nominal thickness is 0.596mm in this study). In order to realize the package reliability of this high bandwidth fcPoP with 4L ETS, the long term reliability test with MSL3A, uHAST 192 hours, TCB 1000 cycles and HTST 1000 hours were performed to show the good yield performance and solderability quality of this low package profile high bandwidth fcPoP. These results show that not only the die size limitations can be overcome by using illustrated finer Cu post interconnections pitch, but also provide the flexibility to allow any memory interface pitch application to stack on this high bandwidth fcPoP. It is believed that the demonstrated enabling technology of high bandwidth fcPoP will be an appropriate and strong 3D packaging solution to achieve highly integrated, miniaturized and low package profile requirements.

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